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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/577,399	05/22/2000	Jun Shi	INTL-0360-US (P8579)	4038

7590 01/14/2005	**EXAMINER**
Timothy N Trop	FAULK, DEVONA E
Trop Pruner & Hu PC	

ART UNIT	PAPER NUMBER
2644	

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DATE MAILED: 01/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
	09/577,399	SHI ET AL.
Office Action Summary	Examiner	Art Unit	
	Devona E. Faulk	2644	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 September 2004*.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Response to Arguments

1.   Applicant's arguments, filed 9/13/2004, with respect to the rejection(s)of claim(s) 1 under 103 (a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of 112 new matter rejection. Note that rejections for claims 1-4 will be forthcoming once the 112 matter is clarified.

2.   Applicant's arguments, filed 9/13/2004, with respect to the rejection(s)of claim(s) 5 under 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Intel's Audio Codec '97 and Fields.

3.   Applicant's arguments, filed 9/13/2004, with respect to the rejection(s)of claim(s) 12 and 17 under 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Intel's Audio Codec '97 and Fields.

Claim Rejections - 35 USC § 112

4.   The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5.   Claims 1-4,6 and 7 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described

in the specification in such a way as to enable one skilled in the art to which it pertains, or with

which it is most nearly connected, to make and/or use the invention. Claims 1 and 6 recite a pair

of analog to digital converters coupled to the third stereo channel pair one of said mixers also

coupled to said pair of analog to digital converters. This indicates that there will be digital

signals from the stereo channel pair going into an analog mixer. It has not been described as to

how an analog mixer will mix a digital signal.

6.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7.   Claims 5-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for

failing to particularly point out and distinctly claim the subject matter which applicant regards as

the invention. Claim 5 recites an audio accelerator coupled to said processor and a codec coupled

to said processor. Although an audio accelerator is mentioned (page 10, line 23) there is no

description of an audio accelerator coupled as claimed.

Claim Rejections - 35 USC § 103

8.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9.   **Claim 5,8,10-13,15,16,20** are rejected under 35 U.S.C. 103(a) as being unpatentable over

Intel Corporation (Audio Codec ,97), hereafter Intel, in view of Fields et al. (U.S. Patent

5,274,708).

Regarding **claim 5**, Intel discloses a processor-based system comprising a processor

(Figure 1; an audio accelerator coupled to said processor; and a codec coupled to said audio

accelerator, said codec including a digital interface including a stereo channel pair and a first pair

of digital -to-analog converters coupled to one of said stereo channel pairs (Figure 1). Intel

further discloses that the digital interface handles multiple input and output audio streams.

Intel's Figure 1 does not specifically disclose a second stereo channel pair and corresponding

D/A converts and analog mixer. The concept of having two stereo channel pairs, two mixers and

having separate outputs for each audio program was well known in the art at the time of filing as

taught by Fields. Fields discloses a digital stereo sound enhancement unit and method (Figure 1)

having two stereo channel pairs (A, B; Figure 1; column 3, lines 60-66) and separate outputs for

each pair (Figure 1). It would have been obvious to one of ordinary skill in the art at the time of

the invention to use Fields's concept of two stereo channel pairs, mixers and to have

corresponding D/A converters in order to provide the capability of outputting separate audio

programs.

Claim 8 claims the processor-based system of claim 5 wherein said system can process

tow separate audio programs at the same time. As stated above apropos of claim 5, the

combination of Intel and Fields meets all elements of that claim. Intel further teaches on page of

23 of an analog signal list comprising a microphone inputs and two CD audio inputs (CD_L, and

CD_R) and two video audio inputs (Video_l and Video_R). The CD audio and the video audio

read on two separate audio programs. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to process two audio programs at the same time for the benefit of increasing the capability of the system.

Claim 10 claims the processor-based system of claim 5 wherein said digital interface includes a plurality of programmable ports so that the connections from the digital interface to said digital-to-analog converters might be changed. As stated above apropos of claim 5, the combination of Intel and Fields meets all elements of that claim. It would have been obvious to one of ordinary skill in the art at the time of the invention to ensure that the digital interface would have a plurality of programmable ports for the benefit of being able to process different types of audio sources.

Claim 11 claims the codec of claim 5 wherein said digital interface has a programmably changeable output data rate. As stated above apropos of claim 5, the combination of Intel and Fields meets all elements of that claim. Intel discloses on page 14 , paragraph 1 that the AC 097 analog component can perform fixed or variable sample rated DAC and ADC conversions. Thus data output from the digital interface can have a programmed changeable output data rate. It would have been obvious to one of ordinary skill in the art to modify Intel's codec so that the digital interface can have a changeable output data rate for the benefit of mixing data.

Regarding **claim 12**, Intel discloses receiving at least one audio program in a codec (Figure 1); converting the audio program to an analog format and mixing the digital program and providing an analog output for each audio program (Figure 1). Intel further discloses that the digital interface handles multiple input and output audio streams. Intel's Figure 1 does not specifically disclose a second stereo channel pair and corresponding D/A converter. The concept

of having two stereo channel pairs, two mixers and having separate outputs for each audio

program was well known in the art at the time of filing as taught by Fields. Fields discloses a

digital stereo sound enhancement unit and method (Figure 1) having two stereo channel pairs (A,

B; Figure 1; column 3, lines 60-66) and separate outputs for each pair (Figure 1). It would have

been obvious to one of ordinary skill in the art at the time of the invention to use Fields's concept

of two stereo channel pairs, mixers and to have corresponding D/A converters in order to provide

the capability of outputting separate audio programs.

Claim 13 claims the method of claim 12 including receiving a third audio program in a

Sony/Phillips digital interconnect format, formatting said third audio program and outputting

said third audio program. As stated above apropos of claim 12, Intel meets all elements of that

claim. Intel further discloses that the digital interface handles multiple input and output audio

streams. Fields teaches of two stereo channel pair outputted separately. It is obvious that if a

third programs were desired it would simply be a design choice to receive a third audio program,

to format it and output it as done with the two digital audio programs. It would have been

obvious to one of ordinary skill in the art at the time of the invention to have the program in a

Sony/Phillips digital interconnect format for the benefit of transmit the data to another device.

Claim 15 claims the method of claim 12 including programmably changing the data rate

of at least one of the said audio programs. As stated above apropos of claim 12, Intel meets all

elements of that claim. Intel discloses on page 14, paragraph 1 that the AC 097 analog

component can perform fixed or variable sample rated DAC and ADC conversions. Thus data

output from the digital interface can have a programmed changeable output data rate. It would

have been obvious to one of ordinary skill in the art to modify Intel's method to include

programmably changing the data rate of at least one of the audio for the benefit of being able to mix data.

Claim 16 claims the method of claim 12 including mixing one of said audio programs in analog format with another analog signal. All elements of claim 16 are comprehended by claim 12.

Regarding **claim 20**, Intel discloses an article comprising a medium storing instructions (that enable a processor-based system to receive at least one digital audio program; convert said digital audio program to an analog format, and programmably change the data rate of at least one of said programs (page 14, paragraph 1). Intel discloses on page 14, paragraph 1 that the AC 097 analog component can perform fixed or variable sample rated DAC and ADC conversions. Thus data output from the digital interface can have a programmed changeable output data rate. Intel's Figure 1 does not specifically disclose a second stereo channel pair and corresponding D/A converts and analog mixer. The concept of having two digital programs and having separate outputs for each audio program was well known in the art at the time of filing as taught by Fields. Fields discloses a digital stereo sound enhancement unit and method (Figure 1) having two stereo channel pairs (A, B; Figure 1; column 3, lines 60-66) and separate outputs for each pair (Figure 1). It would have been obvious to one of ordinary skill in the art at the time of the invention to use Fields's concept of two digital audio programs and to have corresponding D/A converters in order to provide the capability of outputting separate audio programs and obvious to include programmably changing the data rate of at least one of the audio for the benefit of being able to mix data.

10.   **Claim 9** is rejected under 35 U.S.C. 103(a) as being unpatentable over Intel Corporation

(Audio Codec ,97), hereafter Intel, in view of Fields et al. (U.S. Patent 5,274,708) in further

view of Malcolm, Jr. et al. (U.S. Patent 6,301,366).

Claim 9 claims the processor-based system of claim 5 further including a Sony/Phillips

digital interconnect formatter. As stated above apropos of claim 5, the combination of Intel and

Fields meets all elements of that claim. Malcolm discloses a processor-based system including a

Sony/Phillips digital interconnect formatter (Figure 1B). Thus it would have been obvious to

one of ordinary skill in the art at the time of the invention to include a Sony/Phillips digital

interconnect formatter in order to allow the transfer of audio from one file to another without the

conversion to and from an analog format which could degrade signal quality.

11.   **Claims 7,19, and 22** are rejected under 35 U.S.C. 103(a) as being unpatentable over

Intel's Audio Codec in view of Fields et al. (U.S. Patent 5,274,708) in further view of Mayo

(U.S. Patent 5,133,081).

Claim 7 claims the processor-based system of claim 6 wherein said system may

simultaneously play one audio program while recording another audio program. As stated above

apropos of claim 6, the combination of Intel and Fields meets all elements of that claim. Intel

teaches that the Audio Codec '97 has recording capability. Mayo teaches of a system capable of

simultaneously recording and playing messages using the same recording medium (column 10,

lines 42-46). It would have been obvious to one of ordinary skill in the art at the time of the

invention to modify Intel's audio codec by incorporating another codec for the benefit of not

having any interference between the two functions.

Claim 19 claims the article of claim 17 further storing instructions that enable the processor-based system to play one audio program while recording another audio program. As stated above apropos of claim 17, the combination of Intel and Fields meets all elements of that claim. Mayo teaches of a system capable of simultaneously recording and playing messages using the same recording medium (column 10, lines 42-46). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Intel's audio codec by incorporating another codec for the benefit of not having any interference between the two functions.

Claim 22 claims the article of claim 20 further storing instructions that enable the processor-based system to play one audio program while recording another audio program. As stated above apropos of claim 20, the combination of Intel and Fields meets all elements of that claim. Mayo teaches of a system capable of simultaneously recording and playing messages using the same recording medium (column 10, lines 42-46). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Intel's audio codec by incorporating another codec for the benefit of not having any interference between the two functions.

12.   **Claims 14,17-18 and 21** are rejected under 35 U.S.C. 103(a) as being unpatentable over Intel Corporation (Audio Codec ,97), hereafter Intel, in view of Fields et al. (U.S. Patent 5,274,708) in further view of Henderson (U.S. Patent 6,556,539).

Regarding claim 17, Intel discloses an article comprising a medium storing instructions that enable a processor-based system to received at least one digital audio program; convert said digital audio program to an analog format (Figure 1). Intel further discloses that the digital

interface handles multiple input and output audio streams. Intel's Figure 1 does not specifically

disclose a second digital audio program and converting that program to an analog format. The

concept of having two digital audio programs and having separate outputs for each audio

program was well known in the art at the time of filing as taught by Fields. Fields discloses a

digital stereo sound enhancement unit and method (Figure 1) having two stereo channel pairs (A,

B; Figure 1; column 3, lines 60-66) and separate outputs for each pair (Figure 1). It would have

been obvious to one of ordinary skill in the art at the time of the invention to use Fields's concept

of two stereo channel pairs, mixers and to have corresponding D/A converters in order to provide

the capability of outputting separate audio programs. Intel and Fields fail to disclose

programmably changing the assignment of programs to said ports. Henderson discloses the

concept of programmably changing the assignment of programs to ports (column 24, lines 65-

67). It would have been obvious to one of ordinary skill in the art at the time of the invention to

use Henderson's concept of changing the assignment of programs to ports in order to effectively

redesign the system.

Claim 18 claims the article of claim 17 further storing instructions that enable the

processor- based system to programmably change the data rate of at least one of said audio

programs. As stated above apropos of claim 17, Intel meets all elements of that claim. Intel

discloses on page 14, paragraph 1 that the AC 097 analog component can perform fixed or

variable sample rated DAC and ADC conversions. Thus data output from the digital interface

can have a programmed changeable output data rate. It would have been obvious to one of

ordinary skill in the art at the time of the invention to have instructions enabling the codec to

output each the audio programs through a different codec port, programmably changing the

assignment of the ports for the benefit of being able to process different types of audio sources.

Claims 14 and 21 claims the method of claim 12 and the article of claim 20 including

outputting each of said audio programs through a different codec port and programmably

changing the assignment of said programs to said ports. As stated above apropos of claim 12,

the combination of Intel and Fields meets all elements of that claim. Henderson discloses the

concept of changing the assignment of programs to ports (column 24, lines 65-67). It would

have been obvious to one of ordinary skill in the art at the time of the invention to use

Henderson's concept of changing the assignment of programs to ports in order to effectively

redesign the system.

Conclusion

13.   Applicant's amendment necessitated the new ground(s) of rejection presented in this

Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this

final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Devona E. Faulk whose telephone number is 703-305-4359. The examiner can normally be reached on 8 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huyen Le can be reached on 703-305-4844. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DF

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PRIMARY EXAMINER